REPLACEMENT SECTION (CLEAN COPY)

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of the monitoring system according to a preferred embodiment of the present invention.

FIG. 2-00 is another perspective view of the monitoring system according to a preferred embodiment of the present invention.

FIG. 2-01 through FIG. 2-89 provide detailed descriptions of a preferred embodiment of the present invention.

FIG. 3, comprising FIG. 3A, FIG. 3B, FIG. 3C., and FIG. 3D, is a perspective view of a Second logic-processor according to a preferred embodiment of the present invention.

FIG. 4 is a Receiver flowchart according to a preferred embodiment of the present invention.

FIG. 5, comprising FIG. 5A and FIG. 5B, is a perspective view of a power source according to a preferred embodiment of the present invention.

FIG. 6-00 is a perspective view of an electric circuit according to a preferred embodiment of the present invention.

FIG. 6-01 is another perspective view of an electric circuit according to a preferred embodiment of the present invention.

FIG. 7, comprising FIG. 7A, FIG. 7B, FIG. 7C., and FIG. 7D, is a wireless system configurations table according to a preferred embodiment of the present invention.

FIG. 8 is a firmware flowchart according to a preferred embodiment of the present invention.

FIG. 9 is a perspective view of a network coupler according to a preferred embodiment of the present invention.

FIG. 10, comprising FIG. 10A and FIG. 10B, is a sensor sampling-plan according to a preferred embodiment of the present invention.

FIG. 11 is a perspective view of a Second logic-processor according to another preferred embodiment of the present invention.

FIG. 12, comprising FIG. 12A and FIG. 12B, is an alternative perspective view of a Second logic-processor according to a preferred embodiment of the present invention.

FIG. 13, comprising FIG. 13A and FIG. 13B, is a side view of the sections of a Second logic-processor according to a preferred embodiment of the present invention.

FIG. 14, comprising FIG. 14A and FIG. 14B, is a posterior view of the sections of a Second logic-processor for according to a preferred embodiment of the present invention.

Within the specification, reference to a figure number indicates reference to the set of all lettered figures for that number (for example, reference to "FIG. 7" indicates reference to FIG. 7A, FIG. 7B, FIG. 7C., and FIG. 7D).